IN THE CLAIMS

Please cancel claim 16 without prejudice or disclaimer of the subject matter therein.

Please amend claims 1, 7, 15 and 17 as follows:

Sub F1

1. (Currently Amended) A processor comprising:

means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size; and

means for confining the application to a first bit size address space subset, said means for confining comprising:

means for truncating generated address references of the second bit size to the first bit size; and

means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, ~~the~~ <u>a first</u> setting of the address format control signal to ~~determine whether~~ <u>indicate zero-extension of</u> the truncated generated address references ~~are to be zero-extended or sign extended~~ <u>and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references</u>.

2. (Original) The processor of claim 1, wherein the first bit size is 32-bit and the second bit size is 64-bit.

3. (Cancelled)

4. (Previously Presented) The processor of claim 1, wherein the means for confining includes means for generating an address fault.

5. (Original) The processor of claim 1, wherein the means for extending includes means for determining that the first bit size address space subset is signed address space.

6. (Original) The processor of claim 1, wherein the means for extending includes means for determining that the first bit size address space subset is unsigned address space.

7. (Currently Amended) A processor comprising:

a memory to store an instruction of an application ported from a first bit size environment to a second bit size environment, the second bit size being greater than the first bit size; and

an instruction execution core coupled to said memory, said instruction execution core to execute the instruction of the application, said instruction execution core to determine that the application is confined to a first bit size address space subset;

generate an address reference of the second bit size as part of execution of the instruction;

truncate the generated address reference from the second bit size to the first bit size; and

extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on a setting of an address format control signal, ~~the~~ a first setting ~~being used~~ of the address format control signal to ~~determine whether to zero-extend or sign-extend~~ indicate zero-extension of the truncated generated address ~~references~~ reference and a second setting of the address format control signal to indicate sign-extension of the truncated generated address reference.

8. (Original) The processor of claim 7, wherein the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment.

9. (Previously Presented) The processor of claim 7, wherein the instruction execution core is to determine that the application is confined to a first bit size address space subset based at least in part on an address space control flag.

10. (Original) The processor of claim 7, wherein the instruction execution core is to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag.

11. (Previously Presented) The processor of claim 7, wherein the instruction execution core is to generate an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference.

12. (Previously Presented) The processor of claim 11, wherein the instruction execution core is to generate an address fault flag based at least in part on an address fault control flag.

13. (Original) The processor of claim 7, wherein said memory is a cache memory.

14. (Original) The processor of claim 7, wherein the processor is a 64-bit processor.

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15. (Currently Amended) A method ~~to confine an application to an address space subset, the method~~ comprising:

determining that ~~the~~ an application is confined to a first bit size address subset, the application including an instruction;

generating an address reference of a second bit size as part of execution of the instruction;

truncating the generated address reference from the second bit size to the first bit size; and

extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on a setting of an address format control signal, ~~the~~ a first setting ~~being used~~ of the address format control signal to ~~determine whether to zero-extend or sign-extend~~ indicate zero-extension of the truncated generated address ~~references~~ reference and a second setting of the address format control signal to indicate sign-extension of the truncated generated address reference.

16. (Cancelled)

17. (Currently Amended) The method of claim ~~16~~ 15, wherein the application is ported from ~~the first bit size environment to the second bit size environment is an application ported from~~ a 32-bit environment to a 64-bit environment.

18. (Previously Presented) The method of claim 15, wherein determining that an application is confined to a first bit size address subset, the application including an instruction that is based at least in part on an address space control flag.

19. (Original) The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size is based at least in part on an address format control flag.

20. (Original) The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size includes sign-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag.

21. (Original) The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size includes zero-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag.

22. (Previously Presented) The method of claim 15, wherein extending the truncated, generated address reference from the first bit size to the second bit size includes generating an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference.

23. (Previously Presented) The method of claim 22, wherein generating an address fault flag is based at least in part on an address fault control flag.